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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.: 09/754,133 Confirmation No.: 6471

In re Application of:

Yuji YAGI et al. Group Art Unit: 3729

Filed: January 5, 2001 Examiner: Rick Kiltae Chang

For: CIRCUIT BOARD AND SEMICONDUCTOR DEVICE, AND METHOD OF MANUFACTURING THE SAME

APPEAL BRIEF TRANSMITTAL

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Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

November 15, 2004
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BRIEF ON APPEAL

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I. REAL PARTY IN INTEREST

The real party in interest is Matsushita Electric Industrial Co., Ltd. of Osaka, Japan, whose ownership interest is shown in an assignment recorded August 9, 1999 at Reel 10151, Frame 0318.

II. RELATED APPEALS AND INTERFERENCES

A Brief on Appeal was filed September 12, 2003 in this case; prosecution was reopened without a decision on the merits by the Board of Patent Appeals and Interferences. A Request for Reconsideration Under 37 CFR §1.116 was filed April 7, 2004 in reply to an Office Action mailed February 13, 2004. A Final Office Action was mailed July 1, 2004; thereafter a telephone conference on August 16, 2004 was conducted between Examiner Rick K. Chang and appellants' representative, Robert N. Wieland, during which reasons for rejection of the claims were discussed. No agreement was reached.

There is no other appeal or interference known to appellants, the assignee or the undersigned that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

The application is a divisional application under 37 CFR §1.53(b) of application Serial Number 09/332,968, filed June 15, 1999. Claims 1 to 23 were canceled upon filing the present application (those claims were examined in the parent case) and claims 24 to 34 were presented for examination here. Claims 24, 26, 29 and 31 were revised in an Amendment Under 37 CFR §1.111 filed April 8, 2002. Claims 24 to 26 and 29 to 31 were further revised in an Amendment Under 37 CFR §1.116 filed October 7, 2002; that paper was entered when a 37 CFR §1.114 Request for Continued Examination (RCE) was filed November 8, 2002. Claims 24 and 29 were revised and new claims 35 and 36 were added in an Amendment Under 37 CFR §1.111 filed April 30, 2003. Claims 26 to 28 and 31 to 34 stood withdrawn as directed to non-elected species, and claims 24, 25, 29, 30, 35 and 36 were on appeal filed September 12, 2003. Claims 26 to 28 and 31 to 34 stand withdrawn as directed to non-elected species, and claims 24, 25, 29, 30, 35 and 36 are on appeal.

IV. STATUS OF AMENDMENTS

An appeal was taken directly from the Final Rejection. Thus, no amendment is awaiting or has been denied entry. The claims on appeal in the Appendix correspond to the claims that were finally rejected.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention set out in claim 24 on appeal is directed to a method of manufacturing a circuit board 1 including a plurality of wiring patterns 2, each extending across a surface of an insulating substrate 11 for connecting at least two locations on the substrate, and a plurality of protrusions 3 located at desired locations on the wiring patterns; see Figs. 1, 2 and 7. The method includes simultaneously and unitarily forming the wiring patterns and the protrusions (see specification at page 8, lines 21-24 and Figs. 3A-3C).

The limitation "simultaneously and unitarily" (recited in both independent claims 24 and 29) in the context of the claims means forming at one time both wiring patterns and protrusions as a unitized, contiguous single unit, as shown in Figs. 3A-3C.

The limitation "the wiring patterns extending across a surface of an insulating substrate for connecting at least two locations on the substrate" (recited in both independent claims 24 and 29) means the wiring patterns are physically on the surface of the insulating substrate and connect together at least two locations on that surface. See Fig. 1 showing wiring patterns 2 connecting through-hole-electrode 4 at a first location on substrate 11 and a second location on substrate 11 beneath protrusion 3; see also the specification at page 5, line 16 to page 6, line 8.

The invention set out in claim 25, depending from claim 24, on appeal is directed to wiring patterns and the protrusions made of a same conductive sintered material. See the specification at page 8, lines 2-4.

The invention set out in claim 29 on appeal is directed to a method of manufacturing a circuit board 1 including simultaneously and unitarily forming a first plurality of wiring patterns and a second plurality of protrusions located at desired locations on the wiring patterns on an insulating substrate, the protrusions having substantially equal heights (see the specification at page 14, lines 7-11), the wiring patterns each extending across a surface of the substrate for connecting at least two locations on the

substrate; and coupling electrically the protrusions and electrodes disposed on a semiconductor chip component (see the specification at page 14, lines 21-24).

The invention set out in claim 30, depending from claim 29, on appeal is directed to a method wherein the wiring patterns and the protrusions are made of a same conductive sintered material. See the specification at page 8, lines 2-4.

The invention set out in claim 30, depending from claim 24, on appeal is directed to a method further comprising modifying the protrusions to have substantially equal heights. See the specification at page 14, lines 7-11.

The invention set out in claim 36, depending from claim 35, on appeal is directed to a method including imposing a load on said protrusions. See the specification at page 14, lines 7-11.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection before the Board are

(1) claim 24 stands rejected over 35 USC 102(b) as anticipated by Covell, II et al. (U.S. Patent 5,718,367);

(2) claim 25 stands rejected over 35 USC 103(a) as obvious over Covell, II '367 in view of Abe '868;

(3) claims 35-36 stand rejected over 35 USC 103(a) as obvious over Covell, II '367 in view of Abe '868 and Tsunoi (U.S. Patent 6,482,676); and

(4) claims 29-30 stand rejected over 35 USC 103(a) as obvious over of Covell, II '367 in view of Abe '868 and Tsunoi '676.

VII. ARGUMENT

1. Summary of Argument

One of ordinary skill in the art is not directed to the claimed invention from a consideration of either Covell, II '367 alone or a collective consideration of all the cited references. The claims all contain a process treatment feature (simultaneously and unitarily forming wiring patterns and protrusions on a surface of an insulating substrate that connect at least two locations on the substrate) that is neither shown in nor suggested by the cited art. Claims 29 and 35 also call for such protrusions to have substantially equal heights, and claims 25 and 30 also call for the protrusions and wiring patterns to be made of the same conductive sintered material. Such features are not taught or suggested by the cited art.

2. Covell, II '367

The Examiner has asserted (amplified during the August 16, 2004 telephone interview) that Covell, II '367 discloses a method for simultaneously and unitarily forming wiring patterns and protrusions on a surface of a substrate in the same manner as claimed herein. Covell, II '367, Fig. 6 (See Attachment A), shows metal pad 93 attached to semiconductor carrier device 95, and one cylindrical solder portion 70 having a head portion 71 affixed to one pad 93. The Examiner alleges that head portion 71 corresponds to appellants' wiring pattern, and solder portion 70 corresponds to appellants' protrusion. Appellants admit that portions 70 and 71 are formed at the same time, but disagree with the Examiner's argument that head portion 71 corresponds to appellants' wiring pattern and that such wiring pattern connects at least two locations on an insulating substrate.

The Examiner alleges that Covell, II '367, Fig. 4 (see Attachment A), shows pad 93 having a physical width that, in reality would include a pad surface having multiple points of contact (however small, even microscopic) and thereby would meet the requirement in claim 24 that each head portion 71 is a conductor that allegedly functions as a wiring pattern for

connecting multiple locations on an insulating substrate. The Examiner interprets Covell, II '367, Figs. 4 and 5, as showing a single protrusion 70 attaching to alleged wiring pattern 71, which combination 70-71 connects to multiple locations on a single pad 93 on the substrate, where protrusion 70 and alleged wiring pattern 71 are formed at the same time. The Examiner's focus is on multiple points of contact between head portion 71 and pad 93 is misplaced. Pad 93 is a metal conductor, albeit itself located on an insulating substrate. Appellants' claims recite "the wiring patterns extending across a surface of an insulating substrate for connecting at least two locations on the substrate." Head portion 71, alleged to be a wiring pattern, does not extend across substrate 95 (see Fig. 4, Attachment A), but instead contacts metal pad 93. Therefore, whether or not head portion 71 contacts metal pad 93 at multiple locations on the surface of pad 93 is irrelevant, because metal pad 93 is not an insulating substrate.

The Examiner during the noted telephone interview implied that he is unpersuaded by appellants' argument that claims 24 and 29 recite "for connecting at least two locations on the substrate" meant that such two locations are directly on the substrate, such substrate previously recited as an "insulating substrate," whereas

solder head 71 alleged to function as a wiring pattern connects at least two locations (i.e., points on the microscopic rough surface) on metal pad 93, which is not the same thing as an insulating substrate. This issue is discussed in detail in Section 5 (Part A) below.

3. Abe '868

The Examiner has asserted that Abe '868 teaches using a same conductive sintered material for the wiring patterns and the protrusions in wiring patterns 8 and 9, without alleging that such protrusions and wiring patterns are formed simultaneously and unitarily.

4. Tsunoi '676

The Examiner has asserted that Tsunoi '676, Fig. 1B, teaches modifying the protrusions by imposing a load on the protrusions.

Neither Abe '868 nor Tsunoi '676 overcome the deficiencies of Covell, II '367 detailed above. Claims 25, 29, 30, 35 and 36 are patentable that claim 24 is patentable.

5. The Purported Justification of the Rejection

A. The Examiner at 7. on page 4 of the Final Rejection purports to justify the rejections based upon Covell, II '367 by remarking that

> The unfilled mold 23 is injected with solder into the through-hole 25 starting from the bottom. As the solder is continuously injected into the hole, the solder accumulates from the bottom to form the wiring pattern and continuously accumulates to simultaneously and unitarily form the protrusions (72 which is part of 70). Fig. 4 shows that the opposing ends of 71 extend across a surface of 90, an insulating substrate, to connect at least two locations.

The statement "opposing ends of 71 extend across a surface of 90, an insulating substrate, to connect at least two locations" is inaccurate. Actually, Fig. 4 (see Attachment A) shows solder head 71 having a single end connected to a single pad 93, which in turn is on substrate 95, which is attached to base plate 90. Even if the above description is meant to refer to "opposing ends of solder head 71 extend across a surface of substrate 95," such is not true, because solder head 71 has a single end connected only to pad 93, and not to an insulating substrate. Even if the Examiner's wording "opposing ends" refers to, for example, "right" and "left" sides of solder head 71, those "opposing ends" still would be part of a single conductor connecting to the same pad 93, i.e., to a same

single location, and even if thought to connect respective right and left points on metal pad 93, the "opposing ends" still are not connected to at least two locations on insulating substrate 95.

In summary, the Examiner is understood to say, as a basis for rejection of appellants' claims, that solder head 71, which is a single lump having a finite width and thereby having "opposing ends" such as right and left sides of the head, such opposing sides having surface features contacting at respective points on the surface of metal pad 93, itself located on an insulating substrate. And, that any realistic embodiment of solder head 71 in contact with a metal contact (metal pad 93) is a meeting of multiple points because such meeting surfaces would have irregularities of height in the respective surfaces, so that solder head 71 functions as a wiring pattern connecting at least two locations on an insulating substrate, thereby meeting the claim limitation "extending across a surface of an insulating substrate for connecting at least two locations on the substrate."

Appellants submit that the issue of such contact between solder pad 71 and metal pad 93 is inapposite to claims 24 and 29, which recite connecting at least two locations on an insulating substrate. Metal pad 93 is not an insulating substrate.

Appellants further submit that characterizing solder head 71 in contact with metal pad 93 as a wiring pattern 71 connecting multiple locations on pad 93 due to minor surface irregularities at their mating surfaces, is an unjustified strained interpretation of Covell, II '367, given the context of the art, where such solder heads are bonded to metal pads by heat or conductive paste, and the existence of any surface irregularities is irrelevant to such connections.

The rejection and the justification therefore are both improper.

B. The Examiner at 7. on page 4 of the Final Rejection also states:

> The preamble of the [SIC] claim 24 does not further limits [SIC] the body of the limitation "simultaneously and unitarily form the protrusions."

Claim 24 cannot be read independently of its preamble because the preamble recites structural features of the board being manufactured, such features are referred to in the claim, and therefore, the preamble must be read to give meaning to the claim or is essential to point out the invention. See Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 480-81 (CCPA 1951). The preamble

is not a limitation on the claim unless the claim cannot be read independently of the preamble, and in that instance, the preamble must be read to give meaning to the claim or is essential to point out the invention. Such a situation exists here.

VIII. CONCLUSION

For the foregoing reasons, it is respectfully submitted that claims 24, 25, 29, 30, 35 and 36 patentably define over the cited references and the Board is requested to so rule.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

November 15, 2004
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RELATED PROCEEDINGS APPENDIX

Date	Proceeding	Disposition
September 12, 2003 (Brief on Appeal filed)	Appeal	Prosecution reopened

CLAIMS ON APPEAL

24. A method of manufacturing a circuit board comprising a plurality of wiring patterns each extending across a surface of an insulating substrate for connecting at least two locations on the substrate, and a plurality of protrusions located at desired locations on the wiring patterns, the method comprising:

simultaneously and unitarily forming the wiring patterns and the protrusions.

25. The method of manufacturing a circuit board as defined in Claim 24, wherein the wiring patterns and the protrusions are made of a same conductive sintered material.

29. A method of manufacturing a semiconductor device comprising the steps of:

simultaneously and unitarily forming a first plurality of wiring patterns and a second plurality of protrusions located at desired locations on the wiring patterns on an insulating substrate, the protrusions having substantially equal heights, the wiring patterns each extending across a surface of the substrate for connecting at least two locations on the substrate; and

coupling electrically the protrusions and electrodes disposed on a semiconductor chip component.

30. The method of manufacturing a semiconductor device as defined in Claim 29, wherein the wiring patterns and the protrusions are made of a same conductive sintered material.

35. The method of manufacturing a circuit board as defined in claim 24, further comprising modifying the protrusions to have substantially equal heights.

36. The method of manufacturing a circuit board as defined in claim 35, wherein said modifying comprises imposing a load on said protrusions.